3D Charge Coupled Memory Bringing Down the Memory Wall

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Recently, we have proposed a novel 3D integrated Charge Coupled Device (CCD) memory [1, 2] to address the growing need for low power, high speed, high density and low-cost working memories. Desperately needed progress of this well-known power-performance-area-cost (PPAC) trade-off is currently in a cul-de-sac because scaling of classical Dynamic Random Access Memory (DRAM) is nearing the end. New methods of system assembly such as High Bandwidth Memory (HBM) and Die-to-Wafer bonding have realized substantial improvements in bandwidth and power consumption but did little to reduce the cost. Fundamentally the reason is that the underlying memory technology remained unchanged, and DRAM cost-per-bit reduction slowed down significantly already one decade ago. Research groups around the world are racing to find a low-cost alternative that can marry the twin requirement of high capacity and high reliability.

CCD shift registers were invented in 1970 and widely commercially applied in image sensors until 2010. Its operating principle is purely charge-based and shares the extremely well-known classical semiconductor physics of SRAM and DRAM devices. It can therefore operate at high speed, low voltage and unlimited endurance. Proven bit-cost scalable manufacturing technology of 3D-NAND Flash can now be applied to CCD registers (figure 1) to obtain very dense and highly cost-effective 3D CCD memory. The rapid progress being made in oxide semiconductor channel (OSC) materials promises long retention times, which will be required for practical viability.

For an efficient memory macro implementation, individual CCD registers are bundled in blocks and operated in unison (figure 2). Fortunately, modern computer architectures targeting Machine Learning applications have highly predictable memory access patterns, turning the byte-level random access of Von Neuman's general purpose main memory into an unnecessary and unaffordable luxury. 3D CCD memories define a new class of memory that will bring unprecedented cost and capacity benefits.

We will present and discuss the construction and operating principles of OSC-based 3D CCD memories, experimental data obtained from test structures and its application to CXL buffer memories and Compute-near-Memory (CnM).

References

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[3] B. Wang et al., "3D IGZO Charge Coupled Memory DTCO & STCO Analysis for Compute-near-Memory Applications", IEEE International Symposium on Circuits and Systems (ISCAS), 2025.

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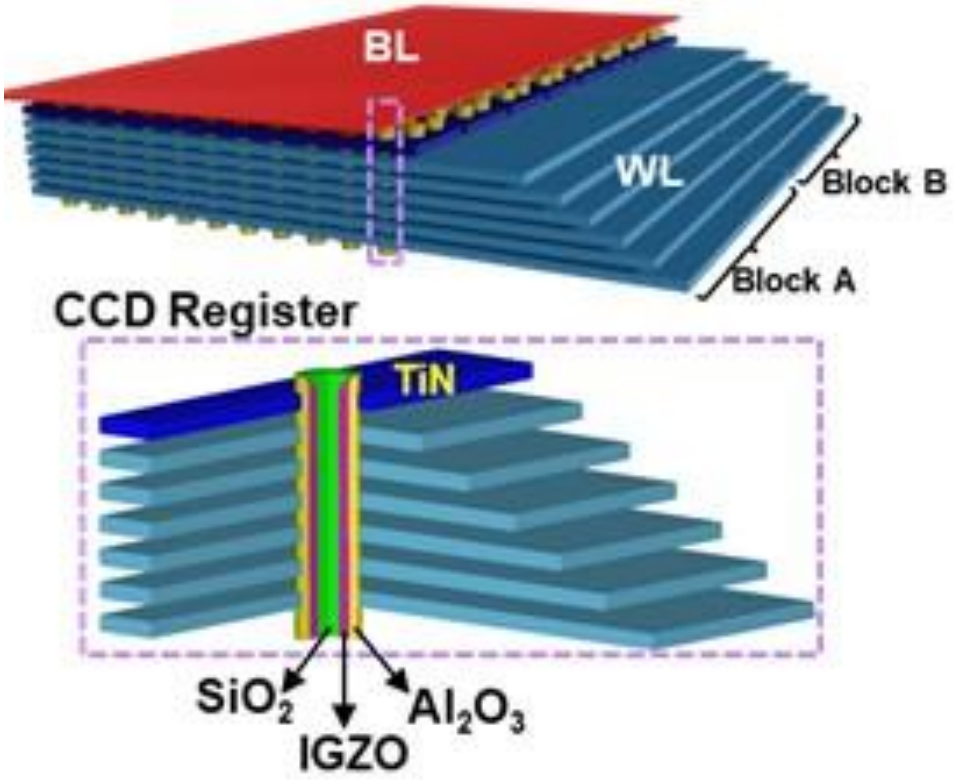

Figure 1: (a) Proposed 3D IGZO-based CCD memory blocks, with an integrated CCD register in vertically aligned plugs and word lines (WL) acting as respective CCD gates; and (b) a cut-in section across a CCD register, exhibiting a string of IGZO MOSCAPs with Al_2O_3 as gate oxide and SiO_2 as filler oxide within the hole punched through the entire stack of gates (cf. [1]).

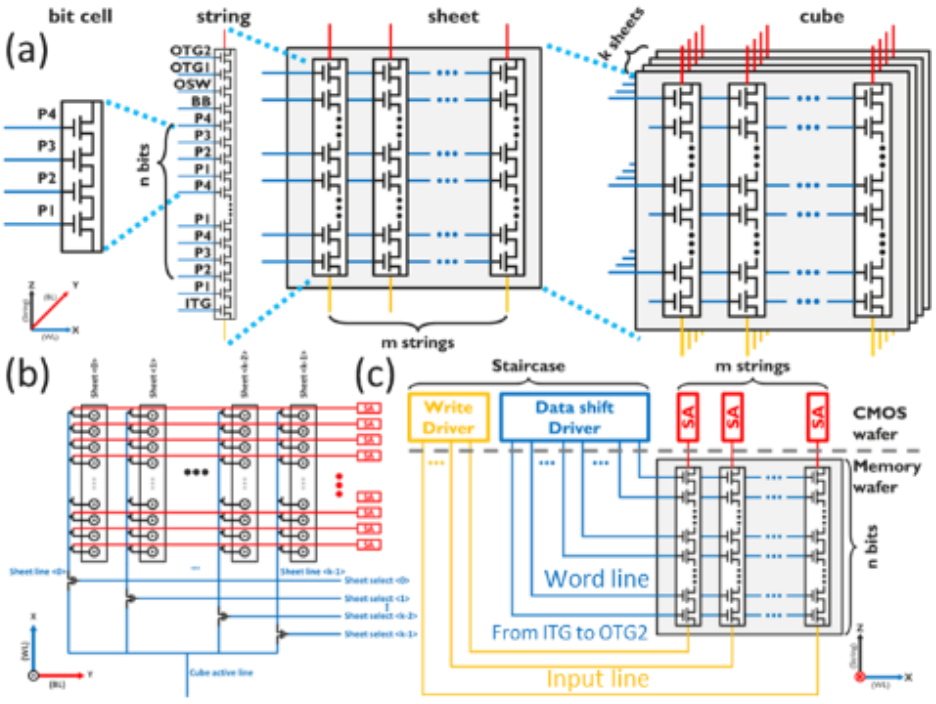

Figure 2: Macro and micro-architecture of the proposed (a) 3D IGZO CCD Memory, (b) multiplexer configuration (top view), (c) 3D heterogeneous integration by Wafer-to-Wafer hybrid bonding (front view) (cf. [3]).